

PATENTS
ALT-256

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicant : Gregory Starr
Application No. : 10/691,152 Confirmation No. : 6613
Filed : October 21, 2003
For : PROGRAMMABLE PHASE-LOCKED LOOP CIRCUITRY
FOR PROGRAMMABLE LOGIC DEVICE
Group Art Unit : 2816

New York, New York 10020
February 2, 2004

Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, applicant hereby makes the following patents and publications of record in the above-identified patent application:

Graham et al. U.S. Patent Re. 35,797 (May 19, 1998)
Wahlstrom U.S. Patent 3,473,160 (October 14, 1969)
Bell et al. U.S. Patent 4,494,021 (January 15, 1985)
Shaw U.S. Patent 4,633,488 (December 30, 1986)
Threewitt et al. U.S. Patent 4,719,593 (January 12, 1988)
Tateishi U.S. Patent 4,857,866 (August 15, 1989)
Popat et al. U.S. Patent 4,868,522 (September 19, 1989)
Podkowa et al. U.S. Patent 4,959,646 (September 25, 1990)
Graham et al. U.S. Patent 5,072,195 (December 10, 1991)
Shizukuishi et al. U.S. Patent 5,075,575 (December 24, 1991)
Ashby et al. U.S. Patent 5,079,519 (January 7, 1992)
Huang U.S. Patent 5,121,014 (June 9, 1992)
Hotta et al. U.S. Patent 5,133,064 (July 21, 1992)
Graham et al. U.S. Patent 5,204,555 (April 20, 1993)
Kersh U.S. Patent 5,208,557 (May 4, 1993)

Norman et al. U.S. Patent 5,239,213 (August 24,
 1993)
 Wright et al. U.S. Patent 5,349,544 (September 20,
 1994)
 Kasturia U.S. Patent 5,394,116 (February 28, 1995)
 West et al. U.S. Patent 5,397,943 (March 14, 1995)
 Nakao U.S. Patent 5,418,499 (May 23, 1995)
 Ishibashi U.S. Patent 5,420,544 (May 30, 1995)
 Fukuda U.S. Patent 5,424,687 (June 13, 1995)
 Meyer U.S. Patent 5,448,191 (September 5, 1995)
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 Hotta et al. U.S. Patent 5,542,083 (July 30, 1996)
 Iga U.S. Patent 5,581,214 (December 3, 1996)
 Mizuno U.S. Patent 5,629,651 (May 13, 1997)
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 Wang et al. U.S. Patent 5,974,105 (October 26, 1999)
 Smith U.S. Patent 5,987,543 (November 16, 1999)
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 Talaga, Jr., et al. U.S. Patent 6,014,048
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 Embree U.S. Patent 6,104,222 (August 15, 2000)
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 Linebarger et al. U.S. Patent 6,141,394
 (October 31, 2000)
 Jeong et al. U.S. Patent 6,144,242 (November 7,
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 Tsai et al. U.S. Patent 6,157,266 (December 5, 2000)
 Wu et al. U.S. Patent 6,249,189 (June 19, 2001)
 Sung et al. U.S. Patent 6,252,419 (June 26, 2001)
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 Friedberg et al. U.S. Patent 6,320,469
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Williams U.S. Patent 6,411,150 (June 25, 2002)
Horan et al. U.S. Patent 6,462,623 (October 8, 2002)
Sung et al. U.S. Patent 6,483,886 (November 19,
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No. 2001/0033188 A1 (October 25, 2001)
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Europe 0 778 517 (June 11, 1997)
Europe 0 987 822 (March 22, 2000)
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Japan 1-137646 (May 30, 1989)
Japan Patent Abstract No. 10,215,156 (August 11,
1998)

Advanced Micro Devices, Inc., "Am2971 Programmable
Event Generator (PEG)," Publication No. 05280, Rev. C,
Amendment /0, pp. 4-286 - 4-303 (July 1986)

Advanced Micro Devices, Inc., "AmPAL*23S8 20-Pin
IMOX PAL-Based Sequencer," Publication No. 06207, Rev. B,
Amendment /0, pp. 4-102 - 4-121 (October 1986)

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1.25/2.0-2.5/3.125 Gbits/s Backplane Interface FPSC,"
Preliminary Data Sheet, pp. 1-35 (July 2001)

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3.3-Volt Digital PLL for CMOS Gate Arrays," Proceedings
of the IEEE 1993 Custom Integrated Circuits Conference,
Publication No. 0-7803-0826-3/93, pp. 23.3.1-23.3.4
(May 9-12, 1993)

LSI Logic Corp., 500K Technology Design Manual
(Document DB04-000062-00, First Edition), pp. 8-1 - 8-33
(December 1996)

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Lucent Technologies, Inc., "ORCA[®] Series 3 Field-Programmable Gate Arrays," Preliminary Data Sheet, Rev. 01 (August 1998)

Monolithic Memories, Inc., "Programmable Array Logic PAL20RA10-20 Advance Information," pp. 5-95 - 5-102 (January 1988)

National Semiconductor Corp., LVDS Owner's Manual & Design Guide (April 25, 1997)

National Semiconductor Corp., "DS90CR285/DS90CR286 +3.3V Rising Edge Data Strobe LVDS 28-Bit Channel Link-66 MHZ," (March 1998)

Xilinx, Inc., "Virtex 2.5V Field Programmable Gate Arrays Advance Product Specification (Version 1.0)" (October 20, 1998)

Xilinx, Inc., "Application Note: Using the Virtex Delay-Locked Loop (Version 1.31)" (October 21, 1998)


Zaks, R., et al., From Chips to Systems: An Introduction to Microcomputers, pp. 54-61 (Prentice-Hall, Inc., Englewood Cliffs, N.J., 1987)

Copies of the aforementioned publications, which are listed on the accompanying Form PTO-1449 (submitted in duplicate), are enclosed herewith.

It is respectfully requested that these patents and publications be (1) fully considered by the Patent and Trademark Office during examination of this application; and (2) printed on any patent which may issue on this application. Applicant requests that a copy of Form PTO-1449, as considered and initialled by the Examiner, be returned with the next communication.

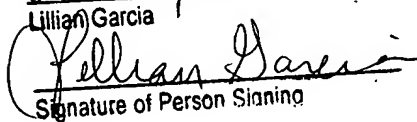
An early and favorable action is respectfully
requested.

Respectfully submitted,



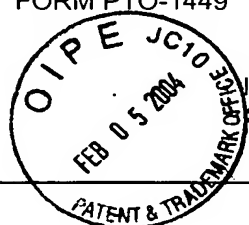
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Lillian Garcia


Signature of Person Signing

FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. AL-256	APPLN. NO. 10/691,152
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICANT Gregory Starr	CONF. NO. 6613
		FILING DATE October 21, 2003	GROUP ART UNIT 2816



U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
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	5,075,575	12/1991	Shizukuishi et al.	307	465	
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	0 416 930	3/1991	European Pat. Off.				
	0 778 517	6/1997	European Pat. Off.				
	0 987 822	3/2000	European Pat. Off.				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

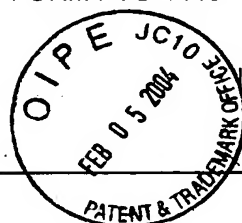
EXAMINER INITIAL	
	Advanced Micro Devices, Inc., "Am2971 Programmable Event Generator (PEG)," Publication No. 05280, Rev. C, Amendment /0, pp. 4-286 - 4-303 (July 1986)
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EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
AL-256APPLN. NO.
10/691,152INFORMATION DISCLOSURE
STATEMENT BY APPLICANTAPPLICANT
Gregory StarrCONF. NO.
6613FILING DATE
October 21, 2003GROUP ART UNIT
2816

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5,121,014	6/1992	Huang	327	276	
	5,133,064	7/1992	Hotta et al.	395	550	
	5,204,555	4/1993	Graham et al.	307	465	
	5,208,557	5/1993	Kersh	331	57	
	5,239,213	8/1993	Norman et al.	326	38	
	5,349,544	9/1994	Wright et al.	364	600	
	5,394,116	2/1995	Kasturia	331	34	
	5,397,943	3/1995	West et al.	326	39	
	5,418,499	5/1995	Nakao	331	57	
	5,420,544	5/1995	Ishibashi	331	11	
	5,424,687	6/1995	Fukuda	331	11	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	1 056 207	11/2000	European Pat. Off.				
	1-137646	5/1989	Japan				
	10,215,156	8/1998	Japan Pat. Abstract				


OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
	DynaChip Corp., "Application Note: Using Phase Locked Loops in DL6035 Devices" (1998)
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	5,506,878	4/1996	Chiang	377	39	
	5,542,083	7/1996	Hotta	709	400	
	5,581,214	12/1996	Iga	331	16	
	5,629,651	5/1997	Mizuno	331	34	
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	5,646,564	7/1997	Erickson et al.	327	158	
	5,656,959	8/1997	Chang et al.	327	105	
	5,691,669	11/1997	Tsai et al.	331	17	
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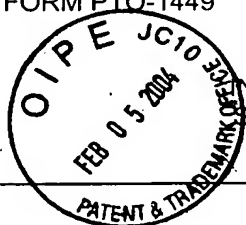
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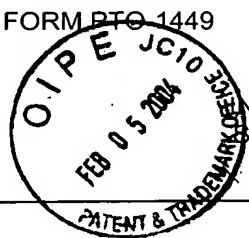
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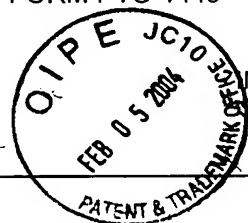
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	Agere Systems, Inc., "ORCA ORT82G5 0.622/1.0-1.25/2.0-2.5/3.125 Gbits/s Backplane Interface FPSC," Preliminary Data Sheet, pp. 1-35 (July 2001)
	Agere Systems, Inc., "ORCA 8850 Field-Programmable System Chip (FPSC) Eight Channel x 850 Mbits/s Backplane Transceiver," Product Brief, pp. 1-6 (July 2001)
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PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
AL-256APPLN. NO.
10/691,152INFORMATION DISCLOSURE
STATEMENT BY APPLICANTAPPLICANT
Gregory StarrCONF. NO.
6613FILING DATE
October 21, 2003GROUP ART UNIT
2816

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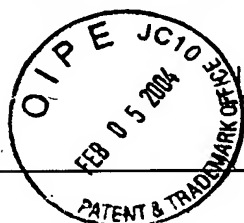
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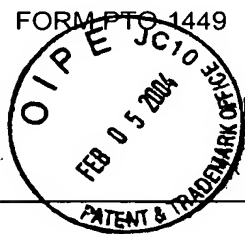
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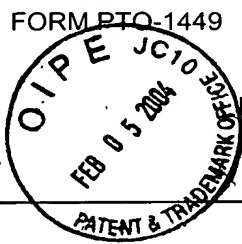
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